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PERFORMANCE EVALUATE OF PARTIALLY DEPLETED AND FULLY DEPLETED SOI MOSFET AT 32 NM TECHNOLOGY

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ABSTRACT

this this paper presents an performance evaluate of partially depleted soi (pdsoi) mosfet and fully depleted soi (fdsoi) mosfet at 32 nm technology. Silicon on insulator (SOI) technology refers for use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing, especially microelectronics, to reduce parasitic device capacitance, thereby improving performance. There are two type of soi mosfet devices pdsoi (partially depleted soi) and fdsoi (fully depleted soi) mosfets. The soi mosfet having silicon junction which is above of an electrical insulator which is silicon dioxide or also known as sapphire, the silicon dioxide is used for short channel effect in microelectronics and sapphire is used for high performance R.F. ad radio sensitive application.

KEYWORDS: — (pdsoi , fdsoi , soi , mosfet.).

INTRODUCTION

Silicon technologies have progress fastest day to day. We must be concentrate on silicon technologies how to effects of reducing the dimension of devices. The scaling down of devices is strongly required to achieve better device performance. Due to reduction in the channel length the short channel effects and leakage current become important issue. To overcome the problem, a new circuit design techniques has been introduce for a newer technologies such as Silicon-on-Insulator (SOI). SOI refers to placing a thin layer of silicon on top of an insulator, usually silicon dioxide (SiO_2) or known as buried oxide layer (BOX). MOSFETs fabricated on SOI substrate that having a relatively thin SOI layer is known as fully depleted SOI and for thick SOI layer is known as partially depleted SOI. Usually, for fully-depleted SOI devices, the thickness of silicon is about less than bulk depletion width. In recent years, silicon-on insulator (SOI) has attracted considerable attention as a for low power application. The quest for scaling down MOSFET size has been going on since its advent due to obvious advantages like speed enhancement, reduction in power consumption and cost.[11] The conventional bulk Si MOSFET has already reached its limit and can't be scaled down any more without compromising any performance metric. Many novel device structures like FinFET, multiple, gate all around (GAA), ultra thin body (UTB) etc have been proposed to continue the scaling down to sub-micron range. Fully depleted substrate is at the heart of all of the above mentioned devices. Fabricating a device on SOI substrate improves performance by reducing parasitic capacitances and various leakage currents. This motivates one to undertake a study of SOI based devices.[11]

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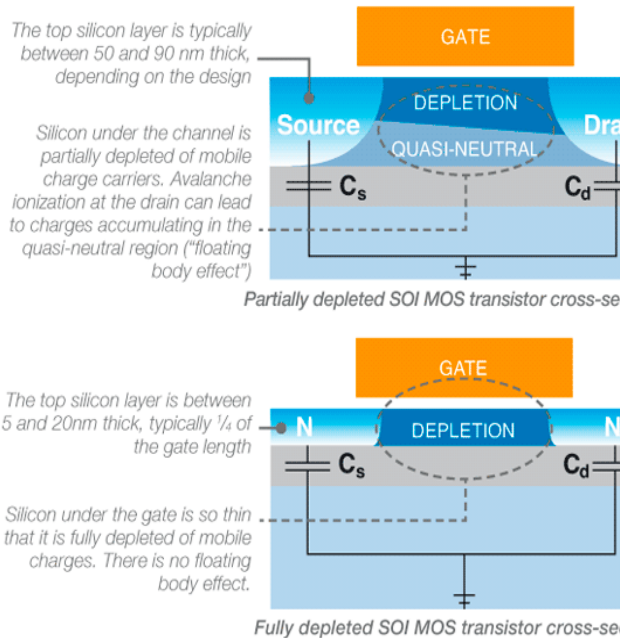

Fig. – Pdsoi And Fdsoi Mosfet

Si body thickness varies for different SOI devices for specific application. [11]A SOI MOSFET with thick Si body is similar to a bulk MOSFET. For such devices the depletion region depth below the gate is smaller than the body thickness and hence the name partially Depleted SOI (pdsoi) MOSFET. SOI devices with very thin Si body (which is fully depleted soi) have better control of gate over channel and thus reduced short channel and floating body effects. In a FDSOI MOSFET the Si substrate being very thin is fully depleted eliminating any floating body effect. Unlike PDSOI, ΨSF is a function of ΨSB. This is shown in the figure below. Only the valence and conduction band edges are shown for simplicity.[11]

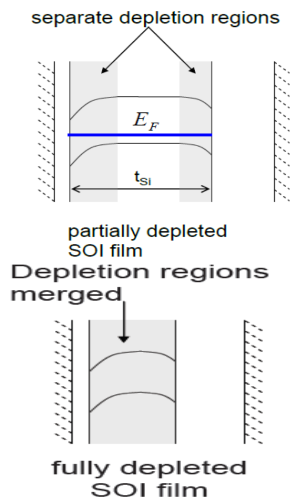

Fig. – Band diagram of PDSOI and FDSOI

Silicon-on-Insulator (SOI)

The desire for higher performance circuits has driven the development of high-speed sub-100 nanometer (nm) silicon-on-insulator (SOI) complementary metal-oxide- semiconductor (CMOS) technology. In SOI technology, metal-oxide semiconductor field-effect transistors (MOSFETs) are formed on a thin layer of silicon overlying a layer of insulating material such as silicon oxide. Devices formed on SOI offer many advantages over their bulk counterparts, including reduced junction capacitance, , soft-error immunity, full dielectric isolation, and absence of latch-up. SOI technology therefore enables higher speed performance and reduced power consumption. We present a system or in other word a method for forming devices on an insulator material. First, a semiconductor depletion material is formed with a predetermined height and width overlying a predetermined portion of the substrate to form an active region. An isolation material formed on top of the substrate surrounding the active region so as to bury a bottom portion of the active region therein, thereby exposing a top portion of the active region. A gate dielectric layer is deposited for covering the exposed the top and two sidewalls of the top portion of the active region, and at least one gate electrode is then formed on top of the gate dielectric layer and extending through two sidewalls thereof to reach the isolation material.[10]

Depending on the silicon film thickness Si , the SOI-MOSFET can be operated in two different modes partially-depleted (PD) and fully-depleted (FD). The device requirements for fabrication are different for each mode. Currently, PD-SOI is favored over FD-SOI, due to manufacturing considerations and other advantages to be explained here, and such a trend may continue. With physical separation between individual devices in ultra-high density CMOS integrated circuits measured in nanometers. The SOI (Silicon-On-Insulator) substrate wafers, as opposed to conventional bulk wafers, not only solve the problem of electrical isolation between adjacent devices but also allow innovative device layouts resulting insignificantly better than in the case of bulk substrates performance of CMOS circuitry. Hence, SOI substrates rapidly become an important element of the advanced silicon IC technology. [8]

Partially and Fully Depleted SOI MOSFET's

If the silicon film (typically 100 nm) on the BOX layer is thicker than the depletion region depth beneath the gate oxide, and "fully depleted (FD) SOI," if the body (silicon film) thickness is thin enough (typically 50nm

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or less) or the doping concentration of the body is low enough to be fully depleted. FDSOI transistors have superior advantages over PD SOI transistors in terms of extremely low sub-threshold swing (<65 mV/decade), no floating-body effects,. However, since FD SOI transistors are even more sensitive to process variation such as the silicon film layer variation resulting in threshold voltage fluctuation, .For such devices the depletion region depth below the gate is smaller than the body thickness and hence the name partially Depleted SOI (PDSOI) MOSFET.

Partially Depleted SOI MOSFET's

Partially depleted silicon-on-insulator (PD-SOI) transistors are used for high-performance applications because they have significantly reduced junction capacitances (the buried oxide (BOX) layer is typically >100 nm thick) and hence increased circuit operating speed compared to other silicon MOSFET like bulk. However, PD-SOI MOSFETs suffer from the "floating-body" effect if the body region is not tied to a bias voltage, then majority carriers generated by impact ionization (when the transistor is in the on state) accumulate in the body region and forward-bias the source junction, effectively lowering VT. This results in an increase in on-state current that is dependent on the transistor operating history.

Fully Depleted SOI MOSFET's

Planar Fully Depleted Silicon on Insulator (FD-SOI) technology relies on an ultra-thin layer of silicon over a Buried Oxide (commonly called Box). Transistors built into this top silicon layer are Ultra-Thin Body devices and have unique, extremely attractive characteristics. Two flavors of buried oxide can be used: standard thickness (typically 145nm thick as classically in volume production PD-SOI digital chips today), or ultra-thin Box, for example 10 or 25nm (UTBOx, Ultra-Thin Buried Oxide).

SOI based on front and back gate biasing FDSOI device can operate in 9 different modes as shown below for an n type MOSFET.[11]

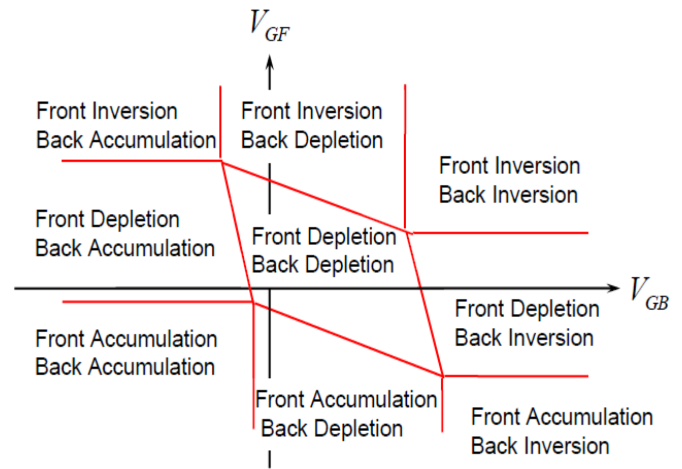

Fig. – Various modes of operation of FDSOI MOSFET

BULK SILICON VERSUS SOI

In general, the body potential of a PD-SOI device may vary during static, dynamic, or transient device operation, and is a function of many factors like temperature, voltage, circuit topology, and switching history. Therefore, circuit design using PD-SOI devices is not straightforward, and there is a significant barrier for the adoption of PD-SOI technology or the migration from bulk-Si design to PD-SOI design .

CONCLUSION AND FUTURE SCOPE

A silicon-on-insulator (SOI) chip is formed with a silicon layer of a predetermined thickness overlying an insulator layer at a predetermined location. A fully-depleted SOI (FD-SOI) device is formed on a first portion of the semiconductor layer using a partially depleted SOI (PD-SOI) technology based process, wherein an active region of the FD-SOI device is isolated and has two top round edges. On the same silicon layer, a partially-depleted SOI (PD-SOI) device is also formed on a second portion of the silicon layer. The SOI devices used for high performance, low power Systems on Chip to ultra-low power applications. This covers markets such as, Mobile Internet Devices (Smartphone's, Tablets, and Net books), Imaging (Digital Camera, Camcorder), Cellular Telecom, Mobile Multimedia, Home Multimedia (Set Top Box, TV, Blu-Ray), etc. We further improved device performance by applying different SOI technology to a block-oxide-enclosed Si body to create a fully depleted silicon-on-insulator (FDSOI) n MOSFET, which overcomes the need for a uniform ultrathin silicon film.

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